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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2129	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,835	NIELL ET AL.	
	Examiner	Art Unit	
	Omar F. Fernández Rivas	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32,34,36 and 38-47* is/are rejected.

7)☐ Claim(s) *33,35,37,48 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *A1, A2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-49 are pending on this application.

Claim Objections

2. Claims 34 and 35 objected to because of the following informalities: both claims recite the same limitations. Appropriate correction is required.

3. Claims 33, 35, 37, 48 and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 26-31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims recite a "data signal flow" which is a form of energy per se that does not fall within one of the four statutory classes of 35 U.S.C. 101 (process, machine, manufacture, or composition of matter).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor et al. in view of Crouse et al. (US Patent #6,532,531, referred to as **O'Connor**; US Patent #4,831,517, referred to as **Crouse**).

Claim 1

O'Connor teaches a memory (**O'Connor**: abstract, L1-3) comprising: a memory array to store data (**O'Connor**: abstract, L1-13; (**O'Connor**: C1, L41-45; Fig. 1); a first pointer coupled to the memory array to address memory locations therein (**O'Connor**: C3, L34-51; C26, L40-62); a pointer memory coupled to the first pointer, the pointer memory to save one or more prior first pointer values of the first pointer (**O'Connor**: C27, L23-43; Examiner's Note (EN): VARS could be a first pointer since it addresses memory locations and is stored in a programmable register (pointer memory). If they are often accessed, they are previous pointer values).

O'Connor does not teach control logic coupled to the pointer memory, the control logic to restore one of the one or more prior first pointer values to the first pointer in response to branch information.

Crouse teaches control logic coupled to the pointer memory, the control logic to restore one of the one or more prior first pointer values to the first pointer in response to branch information (**Crouse**: abstract; C12, L34-68; C13, L1-2; Fig. 7; EN: a program

counter is a pointer to the next instruction to be fetched from memory. BAROA instructions are branch information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of O'Connor by restoring the first pointer value to a prior value as taught by Crouse for the purpose of allowing the pointer to address a previous memory location after a branch instruction has been performed since computer instructions are stored sequentially in memory.

Claim 3

O'Connor does not teach the branch information includes a branch flag to indicate a condition that requires the restoration of the one prior first pointer value to the first pointer.

Crouse teaches the branch information includes a branch flag to indicate a condition that requires the restoration of the one prior first pointer value to the first pointer (**Crouse**: C12, L34-68; C13, L1-2; Fig. 7; EN: an equality signal is a flag included in the branch information. The value of the program counter (first pointer) is restored to the value saved in the register stack (previous value).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of O'Connor by incorporating a flag to indicate that the pointer value should be restored to a previous value as taught by Crouse for the purpose of allowing the system to decide if it should continue reading from the current memory location following the branch instruction or if it should continue

reading from a memory location that was being read before the branch instruction was executed.

Claim 4

O'Connor teaches the branch information is to be received from a processor capable of speculatively issuing requests to read data from the memory array (**O'Connor**: C6, L18-22; C8, L23-31; C18, L47-57; Figs. 1A and 1B).

Claim 5

O'Connor teaches the pointer memory saves a plurality of prior first pointer values as a history of first pointer values (**O'Connor**: C27, L23-43; EN: saving pointers of memory locations often accessed is saving a history of pointer values).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 6-10, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'connor and Crouse as applied to claim 1 above, and further in view of Buckenmaier (US Patent #5,388,074, referred to as **Buckenmaier**).

Claim 2

O'Connor and Crouse do not teach the first pointer is a pop pointer to read data out from the memory array and the memory further comprises, a push pointer to write data into the memory array.

Buckenmaier teaches the first pointer is a pop pointer to read data out from the memory array (**Buckenmaier**: abstract, L12-13; C5, L6-14; Figs. 2,4,5 and 7; EN: a read pointer is a pop pointer as stated in page 1, paragraph 4 of the present Application), and the memory further comprises, a push pointer to write data into the memory array (**Buckenmaier**: abstract, L10-11; C5, L6-14; Figs. 2,4,5 and 7; EN: a write pointer is a push pointer as stated in page 1, paragraph 4 of the present Application).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of O'Connor and Crouse by incorporating a pop pointer and a push pointer as taught by Buckenmaier for the purpose of allowing the system to keep track of the oldest information written and of the next available location into which the next information is to be written (**Buckenmaier**: C1, L44-48).

Claim 6

O'Connor teaches status logic coupled to the pop pointer and the push pointer to monitor a pop pointer value of the pop pointer and a push pointer value of the push pointer to provide an indication of an amount of data stored in the memory array

(**O'Connor**: C3, L19-65; C4, L1-8; C30, L31-58; Fig. 10A; EN: determining the fill and spill condition based on the optop and cache bottom pointers is providing an indication of the amount of data stored in the memory).

Claim 7

The memory of claim 6, wherein the status logic to generate a high status flag in response to an amount of data stored in the memory array being greater than or equal to a high threshold level, and less than or equal to a maximum utilization level (**O'Connor**: C3, L19-65; C4, L1-8; EN: a spill condition is a high status flag).

Claim 8

O'Connor teaches the status logic to further generate a low status flag in response to an amount of data stored in the memory array being less than or equal to a low threshold level and greater than or equal to an empty threshold level (**O'Connor**: C3, L19-65; C4, L1-8; EN: a fill condition is a low status flag).

Claim 9

O'Connor teaches the high threshold level is responsive to the lesser of a maximum branch resolution latency and a low threshold level (**O'Connor**: C3, L19-65, C4, L1-8; C19, L9-16; C19, L46-62; C30, L31-58; Fig. 10A; EN: underflow and overflow are branch resolution latency. The high watermark is a high threshold level).

Claim 10

O'Connor teaches the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory (**O'Connor**: C11, L59-67; C19, L9-16).

Claim 12

The memory of claim 9, wherein the memory array is capable of being directly addressed by a processor to randomly access storage locations therein (**O'Connor**: C3, L5-16; C5, L11-27; EN: pushing and popping data into the memory is accessing storage locations).

Claim 13

O'Connor and Crouse do not teach the memory is a first-in first-out memory.

Buckenmaier teaches the memory is a first-in first-out memory (**Buckenmaier**: abstract, L1-3; C9, claim 1).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of O'Connor and Crouse by using a first-in first-out memory as taught by Buckenmaier for the purpose of having a memory that can handle asynchronous data that can be made available in the order in which it was received (**Buckenmaier**: C1, L55-68).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor and Crouse as applied to claim 1 above, and further in view of Dally et al (US Patent Publication #2003/0070059, referred to as **Dally**).

Claim 11

O' Connor and Crouse do not teach teaches the branch information includes a branch resolution latency, the branch resolution latency is the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the memory.

Dally teaches the branch information includes a branch resolution latency, the branch resolution latency is the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the memory (**Dally**: page 1, paragraph 11).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of O'Connor and Crouse by incorporating a branch resolution latency, the branch resolution latency being the number of instruction cycles to resolve a conditional branch instruction in a processor as

taught by Dally for the purpose of having means to measure the delay in performing a set of instructions in a processor so that improvements can be made to reduce the delay.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 14-17 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckenmaier in view of Crouse et al. (US Patent #5,388,074, referred to as **Buckenmaier**; US Patent #4,831,517, referred to as **Crouse**).

Claim 14

Buckenmaier teaches a method for a first-in first-out (FIFO) memory (**Buckenmaier**: abstract, L1-3), the method comprising: processing one or more pop requests to read data from the FIFO memory (**Buckenmaier**: C1, L44-47; C3, L17-20; C4, L62-64; EN: reading when a read pointer signal is provided is processing a pop request).

Buckenmaier does not teach storing one or more prior pop pointer values of a pop pointer; receiving information to indicate at least one of the one or more pop requests was speculative and a state of the pop pointer of the FIFO memory should be

restored; and restoring one of the one or more prior pop pointer values to the pop pointer in response to the information.

Crouse teaches storing one or more prior pop pointer values of a pop pointer (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next address in memory to read. The prior values are stored in the address register); receiving information to indicate at least one of the one or more pop requests was speculative and a state of the pop pointer of the FIFO memory should be restored (**Crouse**: C2, L21-44; C5, L4-46; EN: Reading from the ROM is a pop request. Returning to the instruction following the patch hook (restoring a state of the pop pointer) if there is no corrective code means that the pop request was speculative) and restoring one of the one or more prior pop pointer values to the pop pointer in response to the information (**Crouse**: abstract; C12, L34-68, C13, L1-2; Fig. 7; EN: BAROA instructions contain the information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating storing prior values of a pop pointer and restoring a previous value of the pop pointer if a pop request was speculative as taught by Crouse for the purpose of allowing the system to recover from an incorrect branch instruction.

Claim 15

Buckenmaier does not teach the one or more prior pop pointer values of the pop pointer are stored into a pointer memory.

Crouse teaches the one or more prior pop pointer values of the pop pointer are stored into a pointer memory (**Crouse**: abstract; C12, L34-68, C13, L1-2; EN: the return address register is a pointer memory where the program counter value (pop counter) is stored).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating storing prior values of the pop pointer in a pointer memory as taught by Crouse for the purpose of having means to retain values of the pointer so that the system can retrieve and use these values when necessary.

Claim 16

Buckenmaier does not teach restoring of the one prior pop pointer value to the pop pointer includes reading the one prior pop pointer value from the pop pointer memory, and loading the one prior pop pointer value into the pop pointer.

Crouse teaches restoring of the one prior pop pointer value to the pop pointer includes reading the one prior pop pointer value from the pop pointer memory, and loading the one prior pop pointer value into the pop pointer (**Crouse**: abstract, L19-27).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating restoring the one prior pop pointer value to the pop pointer includes reading the one prior pop pointer value from the pop pointer memory, and loading the one prior pop pointer value into the pop pointer as taught by Crouse for the purpose allowing the system to fetch

the appropriate pop pointer value so that the pop pointer value can be changed to a value that achieves correct system performance.

Claim 17

Buckenmaier teaches prior to the processing of the one or more pop requests, storing data into a memory array of the FIFO memory, and incrementing a push pointer (**Buckenmaier**: C5, L6-29; C5, L56-61; Figs. 1 and 2; EN: in order to read data from a memory location, data must first be stored in it. Moving a write pointer to the next available register is incrementing a push pointer).

Claim 23

Buckenmaier does not teach bypassing the pop pointer and the push pointer, and directly addressing the memory array of the FIFO memory to read or write data thereto.

Crouse teaches bypassing the pop pointer and the push pointer, and directly addressing the memory array of the FIFO memory to read or write data thereto (**Crouse**: C5, L35-68, C6, L1-2; EN: unconditional branches bypass the push an pop pointers since a memory location different from the one currently addressed by the pop or push pointer is addressed).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of
Buckenmaier by incorporating bypassing the push and pop pointer to directly address

the memory as taught by Crouse for the purpose of not limiting the access to memory to the addresses pointed to by the push and pop pointers.

Claim 24

Buckenmaier teaches loading the pop pointer with an address of the memory array to randomly read data there-from (**Buckenmaier**: C1, L44-47; C5, L6-9; C9, L42-44; Fig 2; EN: making the read pointer address the first stage (memory location) is loading it with an address).

Claim 25

Buckenmaier teaches loading the push pointer with an address of the memory array to randomly write data thereto (**Buckenmaier**: C1, L44-47; C5, L9-10; C9, L38-41; Fig 2; EN: making the write pointer address the second stage (memory location) is loading it with an address).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckenmaier and Crouse as applied to claim 14 above, and further in view of O'Connor (US Patent #6,532,531, referred to as **O'Connor**).

Claim 18

Buckenmaier and Crouse do not teach reading a pop pointer value of the pop pointer and a push pointer value of the push pointer, and determining a status of the memory array in response to the pop pointer value and the push pointer value.

O'Connor teaches reading a pop pointer value of the pop pointer and a push pointer value of the push pointer, and determining a status of the memory array in response to the pop pointer value and the push pointer value (**O'Connor**: C3, L19-65; C4, L1-8; C30, L31-58; Fig. 10A; EN: determining the fill and spill condition based on the optop and cache bottom pointers is determining the status of the memory).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier and Crouse by reading a pop pointer value and a push pointer value for determining the status of the memory as taught by O'Connor for the purpose of comparing the values of these pointers with the total memory available to decide if data can be read or written to a memory location.

Claim 19

Buckenmaier and Crouse do not teach the determining of the status of the memory array is further in response to a high threshold level and a low threshold level.

O'Connor teaches the determining of the status of the memory array is further in response to a high threshold level and a low threshold level (**O'Connor**: C3, L19-65; C4, L1-8; C30, L31-58; Fig. 10A).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier and Crouse by determining the status of the memory based on a high threshold level and a low threshold level as taught by O'Connor for the purpose of having some means to measure when the memory is full or empty to decide if more data can be stored or read from the memory.

Claim 20

Buckenmaier and Crouse do not teach the high threshold level is responsive to the lesser of a maximum branch resolution latency and the low threshold level.

O'Connor teaches the high threshold level is responsive to the lesser of a maximum branch resolution latency and the low threshold level (**O'Connor**: C3, L19-65, C4, L1-8; C19, L9-16; C19, L46-62; C30, L31-58; Fig. 10A; EN: underflow and overflow are branch resolution latency. The high watermark is a high threshold level).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier and Crouse by having a high threshold level responsive to the lesser of a maximum branch resolution latency and a low threshold level as taught by O'Connor for the purpose of deciding if the memory is ready to be read or written to based on whether the memory is busy processing a request or if it has any available memory locations.

Claim 21

Buckenmaier and Crouse do no teach the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory.

O'Connor teaches the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory (**O'Connor**: C11, L59-67; C12, L19-22; C15, L34-40; C19, L9-16).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier and Crouse by having a maximum branch resolution latency be a depth of an instruction pipeline in a processor as taught by O'Connor for the purpose of having means to measure how many instructions are pending to be executed in the processor's pipeline.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buckenmaier, Crouse and O'Connor as applied to claims 18-21 above, and further in view of Dally et al (US Patent Publication #2003/0070059, referred to as **Dally**).

Claim 22

Buckenmaier, Crouse and O'Connor do not teach teaches the branch information includes a branch resolution latency, the branch resolution latency is the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the first-in first-out memory.

Dally teaches the branch information includes a branch resolution latency, the branch resolution latency is the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the first-in first-out memory (**Dally**: page 1, paragraph 11).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier, Crouse and O'Connor by incorporating a branch resolution latency, the branch resolution latency being the number of instruction cycles to resolve a conditional branch instruction in a processor as taught by Dally for the purpose of having means to measure the delay in performing a set of instructions in a processor so that improvements can be made to reduce the delay.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckenmaier in view of Dally et al (US Patent #5,388,074, referred to as **Buckenmaier**; US Patent Publication #2003/0070059, referred to as **Dally**).

Claim 26

Buckenmaier teaches branch resolution latency to determine which one of one or more prior pointer values to restore into a state of a pop pointer (**Buckenmaier**: C2, L17-32; EN: FIFO access time is a branch resolution latency (completion time of a read or write operation)).

Buckenmaier does not teach a branch indicator to indicate that a conditional branch instruction was resolved to take the branch.

Dally teaches a branch indicator to indicate that a conditional branch instruction was resolved to take the branch (**Dally**: page 2, paragraphs 18-21, pages 10-11, claims 1 and 2; EN: the conditional vector operators are branch indicators).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating a branch indicator to indicate that a conditional branch instruction was resolved to take the branch as taught by Dally for the purpose of notifying the system that the conditions to perform a branch has been met.

Claim 27

Buckenmaier does not teach the branch resolution latency is a number indicating how many instruction cycles were executed to resolve a conditional branch instruction in a processor, the processor to couple to the first-in first-out memory

Dally teaches the branch resolution latency is a number indicating how many instruction cycles were executed to resolve a conditional branch instruction in a processor, the processor to couple to the first-in first-out memory (**Dally**: page 1, paragraph 11).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating a branch resolution latency, the branch resolution latency being the number of instruction cycles executed to resolve a conditional branch instruction in a processor as taught by dally for the purpose of having means to measure the delay in performing a set of instructions in a processor so that improvements can be made to reduce the delay.

Claim 28

Buckenmaier does not teach the branch resolution latency is a number indicating a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory.

Dally teaches the branch resolution latency is a number indicating a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory (**Dally**: page 1, paragraph 11; EN: the number of clock cycles to test a

condition will depend on the number of instructions in the test condition (depth of the instruction pipeline)).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by having a maximum branch resolution latency be a depth of an instruction pipeline in a processor as taught by Dally for the purpose of having means to measure how many instructions are pending to be executed in the processor's pipeline.

Claim 29

Buckenmaier teaches a delayed branch indicator to indicate a delay of a branch instruction (**Buckenmaier**: C2, L17-32).

Claim 31

Buckenmaier teaches one or more pop requests to read data from a memory array of the FIFO memory (**Buckenmaier**: C4, L62-64; EN: the read pointer signal is a pop request).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Daniel et al. in view of Dally et al. (US Patent Publication #2001/0047439, referred to as **Daniel**; US Patent Publication #2003/0070059, referred to as **Dally**).

Claim 32

Daniel teaches a first plurality of branch-aware first-in first-out (FIFO) memories to pass data from one processor to the next in a first direction, each branch-aware FIFO memory of the first plurality of branch-aware FIFO memories interleaved between a pair of processors of the plurality of processors (**Daniel**: page 1, paragraph 7, L1-1-12; page 4, paragraph 48, L1-12; page 8, claim 18, L1-5; Figs. 5-8; EN: the writer (first processor) puts data on the FIFO (passes data) for the reader (second processor)). If the FIFO is connected to the processors through the bus, it is interleaved between them); a first input branch-aware FIFO memory coupled to a first processor of the plurality of processors to receive input data in the processing unit (**Daniel**: page 1, paragraphs 9-10; Fig. 2; EN: the FIFO is implemented in the writer module and it receives input data from the writer module); and a first output FIFO memory coupled to a last processor of the plurality of processors to drive output data from the processing unit (**Daniel**: page 4, paragraph 48; Fig. 5; EN: the FIFO resides in the reader module and it outputs data when the reader module performs a read operation).

Daniel does not teach a plurality of processors, each of the processors including an instruction pipeline to speculatively execute instructions before a conditional branch is resolved.

Dally teaches a plurality of processors, each of the processors including an instruction pipeline to speculatively execute instructions before a conditional branch is resolved (**Dally**: page 2, paragraph 13).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by incorporating an instruction pipeline to speculatively execute instructions before a conditional branch is resolved as taught by Dally for the purpose of allowing the processors to guess the outcome of a branch so as to reduce the processor's idle time due to the branch latency period (**Dally**: pages 1 and 2, paragraphs 12 and 13).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Daniel and Dally as applied to claim 32 above, and further in view of Crouse et al. (US Patent #4,831,517, referred to as **Crouse**).

Claim 34

Daniel teaches a memory array to store data (**Daniel**: page 1, paragraph 5; L11-15); a push pointer coupled to the memory array to address memory locations therein to

write data (**Daniel**: page 1, paragraph 11; L1-4; Fig. 2); a pop pointer coupled to the memory array to address memory locations therein to read data (**Daniel**: page 1, paragraph 11; L1-4; Fig. 2).

Daniel and Dally do not teach a pointer memory coupled to the pop pointer, the pointer memory to save one or more prior pop pointer values of the pop pointer; and control logic coupled to the pointer memory, the control logic to restore one of the one or more prior pop pointer values to the pop pointer in response to branch information received from a processor.

Crouse teaches a pointer memory coupled to the pop pointer, the pointer memory to save one or more prior pop pointer values of the pop pointer (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next address in memory to read. The prior values are stored in the address register); and control logic coupled to the pointer memory, the control logic to restore one of the one or more prior pop pointer values to the pop pointer in response to branch information received from a processor (**Crouse**: C2, L21-44; C5, L4-46; EN: Returning to the instruction following the patch hook is restoring the pop pointer value. BAROA instructions contain the information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel and Dally by having a pointer memory to save a prior pop pointer and restoring the first pointer value to a prior value as taught by Crouse for the purpose of allowing the system to restore a pointer to address a previous memory location after returning from a branch instruction to

continue program execution.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 36, 38-39, 41-43 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniel et al. in view of Dally et al. in view of Crouse et al. (US Patent Publication #2001/0047439, referred to as **Daniel**; US Patent Publication #2003/0070059, referred to as **Dally**; US Patent #4,831,517, referred to as **Crouse**).

Claim 36

Daniel teaches a computer system (**Daniel**: page 7, claim 1; EN: a multiprocessor system is a computer system) including: an input/output device (**Daniel**: page 6, paragraph 70, L1-5; EN: disk drives and network peripherals are input/output devices); dynamic random access memory (**Daniel**: page 1, paragraph 8; page 7, claim 11); and a multi-processor coupled to the dynamic random access memory and the input/output device (**Daniel**: page 6, paragraph 70, L1-5; page 7, claim 1; Figs. 5-8); a first plurality of branch-aware first-in first-out (FIFO) memories to pass data from one processor to the next in a first direction, each branch-aware FIFO memory of the first plurality of branch-aware FIFO memories interleaved between a pair of processors of

the plurality of processors (**Daniel**: page 1, paragraph 7, L1-1-12; page 4, paragraph 48, L1-12; page 8, claim 18, L1-5; Figs. 5-8; EN: the writer (first processor) puts data on the FIFO (passes data) for the reader (second processor). If the FIFO is connected to the processors through the bus, it is interleaved between them); a first input branch-aware FIFO memory coupled to a first processor of the plurality of processors to receive input data in the processing unit (**Daniel**: page 1, paragraphs 9-10; Fig. 2; EN: the FIFO is implemented in the writer module and it receives input data from the writer module); a first output FIFO memory coupled to a last processor of the plurality of processors to drive output data from the processing unit (**Daniel**: page 4, paragraph 48; Fig. 5; EN: the FIFO resides in the reader module and it outputs data when the reader module performs a read operation) and wherein each branch-aware FIFO memory includes, a memory array to store data (**Daniel**: page 1, paragraph 5; L11-15), a push pointer coupled to the memory array to address memory locations therein to write data (**Daniel**: page 1, paragraph 11; L1-4; Fig. 2), a pop pointer coupled to the memory array to address memory locations therein to read data (**Daniel**: page 1, paragraph 11; L1-4; Fig. 2).

Daniel does not teach the multi-processor including, a plurality of processors, each of the processors including an instruction pipeline to speculatively execute instructions before a conditional branch is resolved.

Dally teaches the multi-processor including, a plurality of processors, each of the processors including an instruction pipeline to speculatively execute instructions before a conditional branch is resolved (**Dally**: page 2, paragraph 13).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by incorporating an instruction pipeline to speculatively execute instructions before a conditional branch is resolved as taught by Dally for the purpose of allowing the processors to guess the outcome of a branch so as to reduce the processor's idle time due to the branch latency period (**Dally**: pages 1 and 2, paragraphs 12 and 13).

Daniel and Dally do not teach a pointer memory coupled to the pop pointer, the pointer memory to save one or more prior pop pointer values of the pop pointer, and control logic coupled to the pointer memory, the control logic to restore one of the one or more prior pop pointer values to the pop pointer in response to branch information received from a processor.

Crouse teaches a pointer memory coupled to the pop pointer, the pointer memory to save one or more prior pop pointer values of the pop pointer (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next address in memory to read. The prior values are stored in the address register), and control logic coupled to the pointer memory, the control logic to restore one of the one or more prior pop pointer values to the pop pointer in response to branch information received from a processor (**Crouse**: C2, L21-44; C5, L4-46; EN: Returning to the instruction following the patch hook is restoring the pop pointer value. BAROA instructions contain the information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel and Dally by having a

pointer memory to save a prior pop pointer and restoring the first pointer value to a prior value as taught by Crouse for the purpose of allowing the system to restore a pointer to address a previous memory location after returning from a branch instruction to continue program execution.

Claim 38

Daniel teaches a processor comprising: a first branch-aware first-in first-out (FIFO) memory to pass data from the processor to another processor, the first branch-aware FIFO memory to receive branch information responsive to the conditional branch (**Daniel**: page 1, paragraph 7, L1-1-12; page 4, paragraph 48, L1-12; page 7, claim 1; Figs. 5-8; EN: the writer (first processor) puts data on the FIFO (passes data) for the reader (second processor). The FIFO is used for data communication between processors. The branch information is a read or write command), the first branch-aware FIFO memory including a memory array to store data (**Daniel**: page 1, paragraph 5; L11-15), a push pointer coupled to the memory array to address memory locations therein to write data (**Daniel**: page 1, paragraph 11; L1-4; Fig. 2), a pop pointer coupled to the memory array to address memory locations therein to read data (**Daniel**: page 1, paragraph 11; L1-4; Fig. 2).

Daniel does not teach an instruction pipeline to speculatively execute instructions before a conditional branch is resolved.

Dally teaches an instruction pipeline to speculatively execute instructions before a conditional branch is resolved (**Dally**: page 2, paragraph 13).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by incorporating an instruction pipeline to speculatively execute instructions before a conditional branch is resolved as taught by Dally for the purpose of allowing the processors to guess the outcome of a branch so as to reduce the processor's idle time due to the branch latency period (**Dally**: pages 1 and 2, paragraphs 12 and 13).

Daniel and Dally do not teach a pointer memory coupled to the pop pointer, the pointer memory to save one or more prior pop pointer values of the pop pointer, and control logic coupled to the pointer memory, the control logic to restore one of the one or more prior pop pointer values to the pop pointer in response to the branch information.

Crouse teaches a pointer memory coupled to the pop pointer, the pointer memory to save one or more prior pop pointer values of the pop pointer (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next address in memory to read. The prior values are stored in the address register), and control logic coupled to the pointer memory, the control logic to restore one of the one or more prior pop pointer values to the pop pointer in response to the branch information (**Crouse**: C2, L21-44; C5, L4-46; EN: Returning to the instruction following the patch hook is restoring the pop pointer value. BAROA instructions contain the branch information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel and Dally by having a

pointer memory to save a prior pop pointer and restoring the first pointer value to a prior value as taught by Crouse for the purpose of allowing the system to restore a pointer to address a previous memory location after returning from a branch instruction to continue program execution.

Claim 39

Daniel and Dally do not teach teaches the branch information includes a branch flag to indicate a condition requiring restoration of the one prior pop pointer value to the pop pointer.

Crouse teaches the branch information includes a branch flag to indicate a condition requiring restoration of the one prior pop pointer value to the pop pointer (**Crouse**: C12, L34-68; C13, L1-2; Fig. 7; EN: an equality signal is a flag included in the branch information. The value of the program counter (first pointer) is restored to the value saved in the register stack (previous value).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel and Dally by incorporating a flag to indicate that the pointer value should be restored to a previous value as taught by Crouse for the purpose of allowing the system to decide if it should continue reading from the current memory location following the branch instruction or if it should continue reading from a memory location that was being read before the branch instruction was executed.

Claim 41

The processor of claim 38, further comprising: status logic coupled to the pop pointer and the push pointer to monitor a pop pointer value of the pop pointer and a push pointer value of the push pointer to provide an indication of an amount of data stored in the memory array (**Daniel**: page 1, paragraph 11; page 2, paragraphs 15 and 17; page 7, claim 1; EN: comparing the values of the pointers to determine if the FIFO is full or empty is providing an indication of the amount of data stored).

Claim 42

The processor of claim 41, wherein the status logic to generate a high status flag in response to an amount of data stored in the memory array being greater than or equal to a high threshold level, and less than or equal to a maximum utilization level (**Daniel**: page 1, paragraph 11; page 2, paragraph 15; page 2, paragraphs 17-18 and 23-25; EN: returning a code of 0 if the FIFO is full is generating a high status flag).

Claim 43

The processor of claim 41, wherein the status logic to further generate a low status flag in response to an amount of data stored in the memory array being less than or equal to a low threshold level and greater than or equal to an empty threshold level (**Daniel**: page 1, paragraph 11; page 2, paragraph 15; pages 1 and 2, paragraphs 12-15 and 21-22; EN: returning a code of 0 if the FIFO is empty is generating a low status flag).

Claim 46

Daniel and Crouse do not teach the branch information includes a branch resolution latency, the branch resolution latency is the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the memory.

Dally teaches the branch information includes a branch resolution latency, the branch resolution latency is the number of instruction cycles to resolve a conditional branch instruction in a processor, the processor to couple to the memory (**Dally**: page 1, paragraph 11).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel and Crouse by incorporating a branch resolution latency, the branch resolution latency being the number of instruction cycles executed to resolve a conditional branch instruction in a processor as taught by Dally for the purpose of having means to measure the delay in performing a set of instructions in a processor so that improvements can be made to reduce the delay.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 40, 44-45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniel, Dally and Crouse as applied to claims 36, 38-39, 41-43 and 46 above, and further in view of O'Connor et al. (US Patent #6,532,531, referred to as **O'Connor**).

Claim 40

Daniel, Dally and Crouse do not teach the pointer memory saves a plurality of prior pop pointer values as a history of pop pointer values.

O'Connor teaches the pointer memory saves a plurality of prior pop pointer values as a history of pop pointer values (**O'Connor**: C27, L23-43; EN: saving pointers of memory locations often accessed is saving a history of pointer values).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel, Dally and Crouse by incorporating a pointer memory to save prior pop pointers as a history of pop pointer values as taught by O'Connor for the purpose of allowing the system to revert back to a previous value of the pop pointer if required by an instruction.

Claim 44

Daniel Dally and Crouse do not teach the high threshold level is responsive to the lesser of a maximum branch resolution latency and a low threshold level.

O'Connor teaches the high threshold level is responsive to the lesser of a maximum branch resolution latency and a low threshold level (**O'Connor**: C3, L19-65,

C4, L1-8; C19, L9-16; C19, L46-62; C30, L31-58; Fig. 10A; EN: underflow and overflow are branch resolution latency. The high watermark is a high threshold level).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel, Dally and Crouse by incorporating a high threshold level responsive to a maximum branch resolution latency and a low threshold level as taught by O'Connor for the purpose of having means to determine the status of the memory (full or empty).

Claim 45

Daniel and Crouse do not teach the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory.

Dally teaches the maximum branch resolution latency is a depth of an instruction pipeline in a processor, the processor to couple to the first-in first-out memory (**Dally**: page 1, paragraph 11; EN: the number of clock cycles to test a condition will depend on the number of instructions in the test condition (depth of the instruction pipeline)).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel and Crouse by having a maximum branch resolution latency be a depth of an instruction pipeline in a processor as taught by Dally for the purpose of having means to measure how many instructions are pending to be executed in the processor's pipeline.

Claim 47

Daniel, Dally and Crouse do not teach the memory array is capable of being directly addressed to randomly access storage locations therein.

O'Connor teaches the memory array is capable of being directly addressed to randomly access storage locations therein (**O'Connor**: C3, L5-16; C5, L11-27; EN: pushing and popping data into the memory is accessing storage locations).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Daniel, Dally and Crouse by incorporating a memory array capable of being directly addressed to randomly access storage locations as taught by O'Connor for the purpose of allowing the computer to read from memory locations specified by the instructions.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hanawa et al. US Patent #6,078,983

Tran et al. US Patent #6,269,436

28. Claims 1-32, 34, 36 and 38-47 are rejected.

Correspondence Information

29. Any inquires concerning this communication or earlier communications from the examiner should be directed to Omar F. Fernández Rivas, who may be reached Monday through Friday, between 8:00 a.m. and 5:00 p.m. EST. or via telephone at (571) 272-2589 or email omar.fernandezrivas@uspto.gov.

If you need to send an Official facsimile transmission, please send it to (571) 273-8300.

If attempts to reach the examiner are unsuccessful the Examiner's Supervisor, David Vincent, may be reached at (571) 272-3080.

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Friday, June 23, 2006

DAVID VINCENT
SUPERVISORY PATENT EXAMINER

OFR